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EP 0264918 A2 WO 95/19658 A WO 94/16428 A
US 5170158 A

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(54) Abstract Title
Digital-type liquid crystal display panel driving circuit

(57) A digital-type liquid crystal display panel driving circuit 40 that drives a liquid crystal panel 30 with a digital image signal to display a picture on the liquid crystal panel. The driving circuit 40 is provided with a storage device array 42,44 for temporarily storing n picture element data imputed thereto, a multiplexor array 46 for selecting k picture element data from the n picture element data stored in the storage device array, a digital to analog converter array 48 for sequentially converting the selected k picture element data from the multiplexor array 46 into k analog picture element signals, and a demultiplexor array 54 for selecting k of n data lines of the liquid crystal display panel 30 and delivering the k analog picture element signals to the selected k data lines. The driving simplifies the circuit configuration and reduces the waste of instantaneous power.

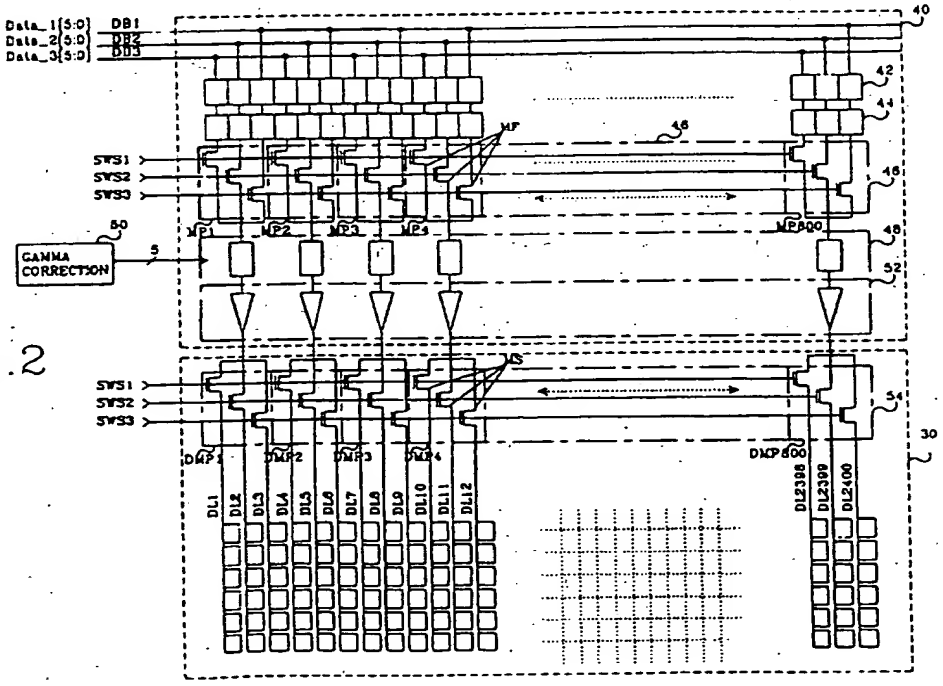

Fig.2

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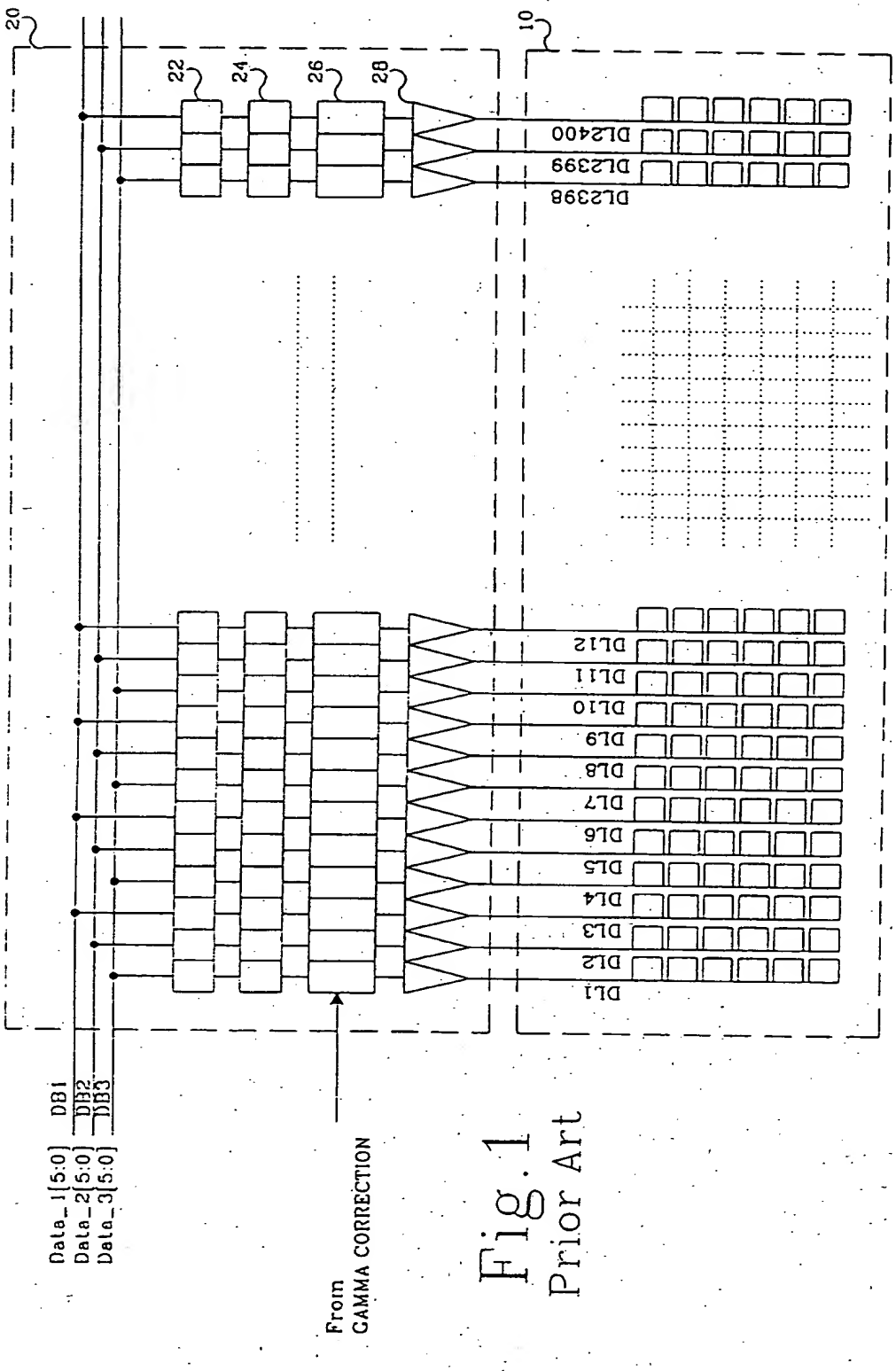
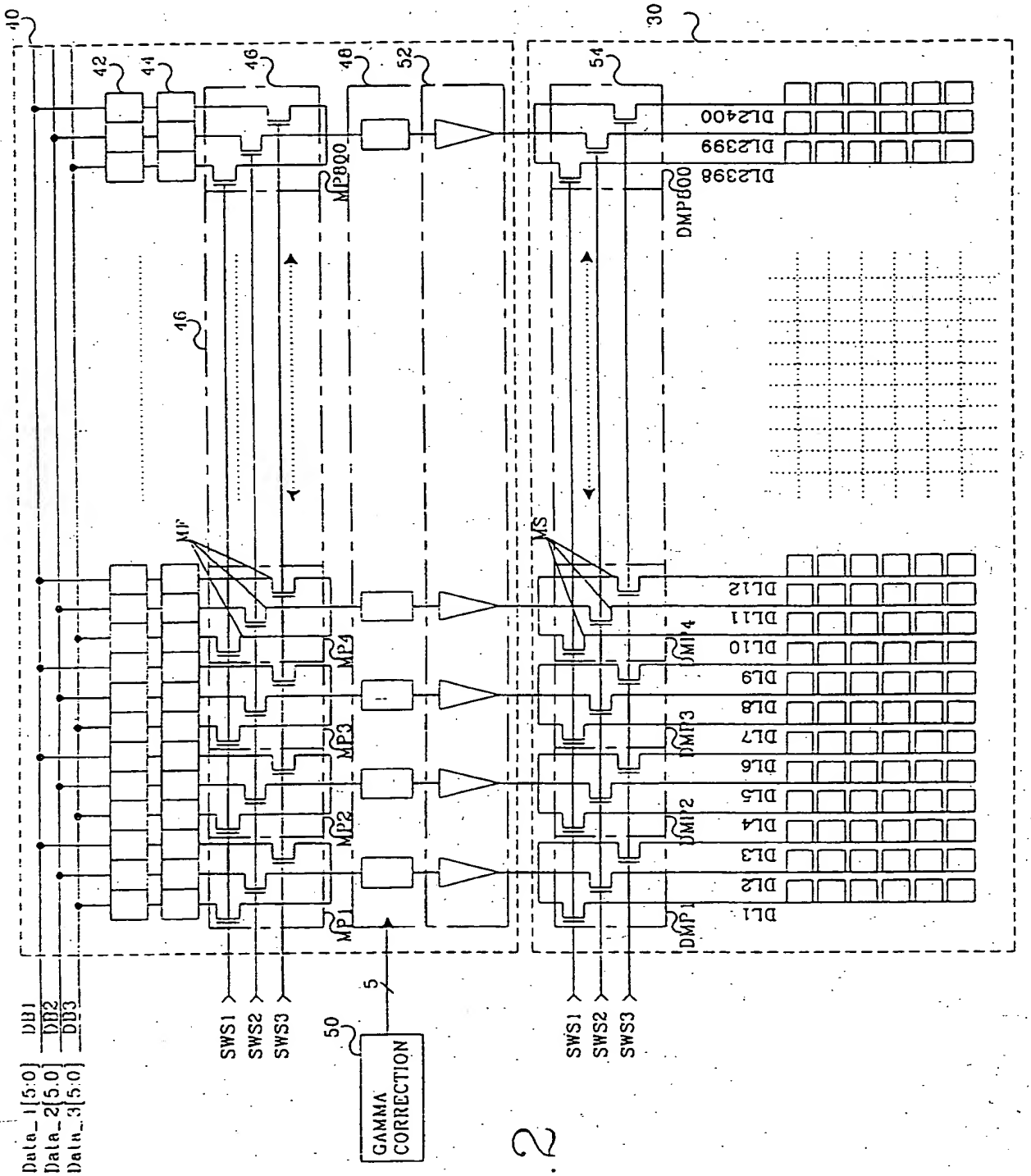


Fig.1
Prior Art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MP4
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MP2
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Fig. 2

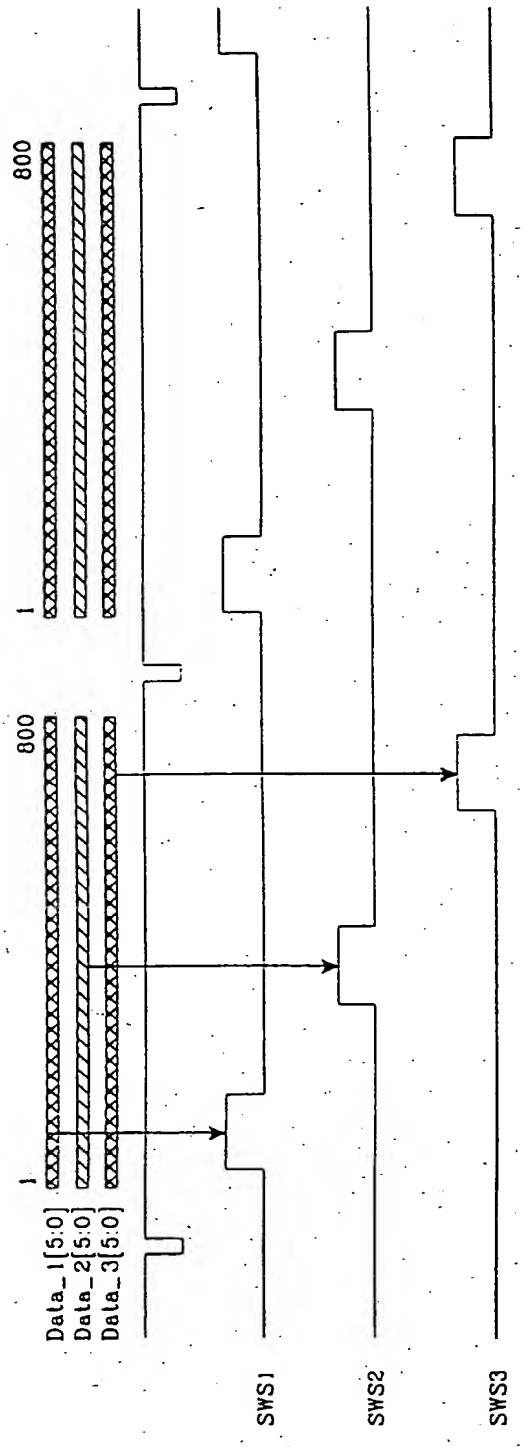

Fig.3

DIGITAL-TYPE LIQUID CRYSTAL DISPLAY PANEL DRIVING CIRCUIT

This invention relates to a display apparatus employing a liquid crystal panel, and more particularly to a digital-type liquid crystal display panel driving circuit that drives the liquid crystal panel with a digital image signal.

Recently, in the image media, there has been a trend toward the use of digital, as opposed to analog, image signals. Digital image signals can be more easily compressed, providing a high resolution picture to a viewer. As a result, it became desirable for liquid crystal displays to be driven by analog as well as digital image signals. Accordingly, the driving circuit for the liquid crystal display panel has been configured to be adaptable for driving picture elements or pixels in a liquid crystal panel requiring an analog signal. As a result, analog-type liquid crystal display driving circuits have come to coexist with digital-type liquid crystal display driving circuits.

Such liquid crystal display panel driving circuits must be able to accurately apply a voltage corresponding to an image signal to each picture element in the liquid crystal display panel for a sufficient time. To this end, in the analog-type liquid crystal display panel driving circuit,

the alternative of sequentially driving picture elements in one horizontal scanning interval by at least two constant number units was disclosed in Japanese Laid-open Patent Publication No. Puyng 7-181933, published on July 21, 1995 and filed by Casio Co, Ltd. In this Japanese patent, an analog-type liquid crystal display panel driving circuit delays an image signal by means of the delay device, and sequentially applies the delayed image signal to picture elements extending from the center of the horizontal line to the right end thereof while applying the undelayed image signal to picture elements extending from the left end of the horizontal line to the center thereof. Such an analog-type liquid crystal display panel driving circuit could secure a sufficient signal supplying time for each of the picture elements even when it sequentially drove the picture elements in the horizontal line by the two number units because it utilized the analog image signal itself as a driving voltage. Otherwise, a digital-type liquid crystal display panel driving circuit can not secure a sufficient signal supplying time for each of the picture elements by the analog-type liquid crystal display panel driving scheme as disclosed in the Japanese patent because it requires time to convert the digital image signal into an analog image signal. Accordingly, the digital-type liquid crystal display panel driving circuit is configured to drive picture elements in one horizontal line, as shown in Fig. 1.

Referring to Fig. 1, a liquid crystal display panel 10 includes 2400 data lines DL1 to DL2400 connected to 600 picture elements arranged in the horizontal direction, respectively. A driving circuit 20 for driving 600 × 2400

number of picture elements in the liquid crystal display panel 10 includes a first latch array 22 connected to the first to third data buses DB1 to DB3, a second latch array 24 cascade-connected to the first latch array 22, a digital to analog (D-A) converter array 26, and an output amplifier array 28. The first and second latch arrays 22 and 24 each consist of 2400 latches. The 2400 latches included in the first latch array 22 are divided into three units of 800 latches each, the units being separately connected to the first to third data buses DB1 to DB3. Further, the 2400 latches included in the first latch array 22 are sequentially driven for the three units to input red(R), green(G) and blue(B) picture elements for a single horizontal line from the first to third data buses DB1 to DB3. Meanwhile, the 2400 latches included in the second latch array 24 receive picture element data from the 2400 latches in the first latch array 22 and deliver it to the D-A converter array 26, respectively. Accordingly, the D-A converter array 26 converts all the element data from the second latch array 24 into picture element signals and applies the converted 2400 picture element signals to the output amplifier array 28. To this end, the D-A converter array 26 consists of 2400 D-A converters commonly inputting a certain number (e.g., five) of converting source signals from a gamma correction portion not shown. These respective 2400 D-A converters generate picture element signals by adding a part of or all of the converting source signals in accordance with a logical value of the picture element data from the corresponding latch of the second latch array 24. Finally, the output amplifier array 28 amplifies the 2400 picture element signals from the D-A converter array 26 at a constant amplification ratio, and

distributively applies the amplified 2400 picture signals to the 2400 data lines DL1 to DL2400 of the liquid crystal display panel 10. To this end, the output amplifier array 28 also comprises 2400 output amplifiers which are distributively connected to the 2400 D-A converters in the D-A converter array 26, respectively.

As described above, the conventional digital-type liquid crystal display panel driving circuit can secure a sufficient signal supplying time for every picture element by simultaneously driving the picture elements for one horizontal line in the liquid crystal panel. In the conventional digital-type liquid crystal display panel driving circuit, however, since it employs D-A converters and output amplifiers which respectively correspond to the number of picture elements included in the horizontal line of the liquid crystal display panel, the circuit configuration thereof is not only complicated, but also large in size. Also, in the conventional digital-type liquid crystal display panel driving circuit, a large number of D-A converters and output amplifiers must be simultaneously driven, wasting instantaneous power.

Accordingly, it is an object of the present invention to provide a digital-type liquid crystal display panel driving circuit with a simplified circuit configuration that reduces the waste of instantaneous power.

It is another object of the present invention to provide a digital-type liquid crystal display panel driving circuit which can reduce the number of lead lines in the liquid

crystal display panel.

In order to attain these and other objects of the invention, a digital-type liquid crystal display panel driving circuit according to the present invention includes a multiplexor array for selecting k digital picture element data from n digital picture element data, a digital to analog converter array for converting the k digital picture element data from the multiplexor array into k analog picture element signals, and a demultiplexor array connected to n data lines for selecting k of the n data lines and for transferring the k analog picture element signals from the digital to analog converter onto the selected k data lines.

A method for driving a digital-type liquid crystal display panel according to the present invention includes the steps of selecting k digital picture element data from n digital picture element data, converting the k digital picture element data from the multiplexor array into k analog picture element signals, selecting k of n data lines, and transferring the k analog picture element signals from the digital to analog converter onto the selected k data lines.

For a better understanding of the present invention, an embodiment will now be described by way of example, with reference to the accompanying drawings, in which:

Fig. 1 shows a configuration of a liquid crystal display apparatus employing the conventional liquid crystal display panel driving circuit for a digital image signal;

Fig. 2 shows a configuration of a liquid crystal display apparatus employing a digital-type liquid crystal display panel driving circuit according to an embodiment of the present invention; and

Fig. 3 is a operation timing diagram of each part of the driving circuit shown in Fig. 2.

Referring to Fig 2, there is shown a liquid crystal display apparatus that includes a digital-type liquid crystal display panel driving circuit according to an embodiment of the present invention. In Fig. 2, the liquid crystal display apparatus comprises a liquid crystal display panel driving circuit 40 connected to a liquid crystal display panel 30. The liquid crystal display panel 30 comprises 2400 data lines DL1 to DL2400 that are commonly connected to 600 picture elements arranged in the vertical direction, respectively.

The driving circuit 40 for driving 600 × 2400 picture elements in the liquid crystal display panel 30 includes a first latch array 42 connected to the first to third data buses DB1 to DB3, a second latch array 44 cascade-connected to the first latch array 42, a multiplexor array 46, and a D-A converter array 48. The first and second latch arrays 42 and 44 each consist of 2400 latches. The 2400 latches included in the first latch array 42 are divided into three units of 800 latches each, the units being separately connected to the first to third data buses DB1 to DB3. Further, the 2400 latches included in the first latch array 42 are sequentially driven for the three units to receive R, G, and B picture element data

for one horizontal line from the first to third data buses DB1 to DB3. Meanwhile, 2400 latches included in the second latch array 44 receive picture element data from the 2400 latches in the first latch array 42 simultaneously, and deliver the same to the multiplexor array 46, respectively.

The multiplexor array 46 divides the 2400 picture element data from the second latch array 44 into three units 800 latches each and delivers the same to the D-A converter array 48 three times. To this end, the multiplexor array 46 consists of 800 multiplexors MP1 to MP800 for receiving the first to third switching control signals SWS1 to SWS3 from the first to third control lines SL1 to SL3, respectively. Each of these 800 multiplexors transfers picture element data from the three latches in the second latch array 44 sequentially to the D-A converter array 48 using the first to third switching control signals SWS1 to SWS3. The first to third switching control signals SWS1 To SWS3 sequentially have a logical value of "1" during one horizontal period, as shown in Fig. 3.

Each of the 800 multiplexors MP1 to MP800 is comprised of three groups of MOS transistors MF for distributively inputting the first to third switching control signals SWS1 to SWS3 to the gates thereof. Note, however, that there should three groups of 5 MOS transistors MF (for a total of 15 MOS transistors MF) in the case of 5-bit picture element data. The sources of these three groups of MOS transistors MF included in a single multiplexor MP are connected to the three latches included in the second latch array 44, respectively, while the drains of the three groups of MOS transistors are commonly connected with respect to each bit of the picture element data.

Further, the three groups of MOS transistors MF included in a single multiplexor MP are sequentially turned on during one horizontal interval by the first to third switching control signals SWS1 to SWS3 to transfer the picture element data from the corresponding latch in the second latch array 44 to the D-A converter array 48. Accordingly, the D-A converter array 48 converts all of the 800 picture element data from the multiplexor array 46 into picture element signals. To this end, the D-A converter array 48 is comprised of 800 D-A converters for commonly receiving a constant number (e,g., at least five) of converting source signals from a gamma correction portion 50. Each of these 800 D-A converters converts the picture element data into analog picture element signals by selectively adding either a part of or the entire of a certain number of converting source signals from the gamma correction portion 50 in accordance with a logical value of the picture element data from the corresponding multiplexor MP. As a result, each of the 800 D-A converters converts three picture element data into analog picture element signals during a single horizontal scanning interval.

The driving circuit 40 also includes an output amplifier array 52 and a demultiplexor array 54 which are seriall connected between the D-A converter array 48 and the data lines DL1 to DL2400 of the liquid crystal display panel 30. The output amplifier array 52 amplifies the 800 picture element signals from the D-A converter array 48 at a certain amplification ratio and outputs the amplified 800 picture element signals to the demultiplexor array 54. To this end, the output amplifier array also is comprised of 800 output amplifiers distributively connected to the 800

D-A converters of the D-A converter array 48. Finally, the demultiplexor array 54 sequentially transfers the 800 amplified picture element signals from the output amplifier array 52 onto the 2400 data lines DL1 to DL2400 three times. To this end, the demultiplexor 54 is comprised of 800 demultiplexors DMP1 to DMP800 for receiving the first to third switching control signals SWS1 to SWS3 from the first to third control lines SL1 to SL3, respectively. Each of these 800 demultiplexors DMP1 to DMP800 sequentially transfers the picture element signals from the output amplifier array 52 to three data lines DL by the first to third switching control signals SWS1 to SWS3 which have a logical value of "1" sequentially during one horizontal interval, as shown in Fig. 3. To this end, each of the 800 demultiplexors DMP1 to DMP800 is comprised of three MOS transistors MS for distributively receiving the first to third switching control signals SWS1 to SWS3 to the gate thereof. The sources of the three MOS transistors MS included in a single demultiplexor DMP are commonly connected to the output terminal of one output amplifier included in the output amplifier array 52, and their drains are distributively connected to three data lines DL. Further, the MOS transistors MS included in one demultipexor DMP are sequentially turned on during one horizontal interval by the first to third switching control signals SWS1 to SWS3 to thereby distributively apply the corresponding output amplifier included in the output amplifier array 52 to the three data lines DL.

As described above, the liquid crystal panel driving circuit of digital type according to the present invention can reduce the number of both the D-A converters and the

output amplifiers into a half or one-third the number of data lines, by providing the multiplexor array between the latch array for temporarily storing the picture element data for one line and the D-A converter array for converting the picture element data into the picture element signal, and by providing the demultiplexor between the output amplifier array and the data lines of the liquid crystal display panel. Accordingly, the digital-type liquid crystal panel driving circuit according to the present invention not only simplifies the circuit configuration, but also reduces the amount of wasted instantaneous power. Also, it reduces the number of lead lines in the liquid crystal display panel by mounting the demultiplexor in the liquid crystal display panel.

Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.

CLAIMS:

1. A digital-type liquid crystal display panel driving circuit, comprising:

a multiplexor array for selecting k digital picture element data from n digital picture element data;

a digital to analog converter array for converting the k digital picture element data from the multiplexor array into k analog picture element signals; and

a demultiplexor array connected to n data lines for selecting k of the n data lines and for transferring the k analog picture element signals from the digital to analog converter onto the selected k data lines.

2. The digital-type liquid crystal display panel driving circuit of claim 1 further including:

a liquid crystal display panel having n data lines arranged in parallel in a horizontal direction, said n data lines being commonly connected to m picture elements arranged in a vertical direction.

3. The digital-type liquid crystal display panel driving circuit of claim 1 or 2, wherein said demultiplexor array is loaded in said liquid crystal display panel.

4. The digital-type liquid crystal display panel driving circuit of claim 1, 2 or 3, further including:

a storage device array for temporarily storing n digital picture element data inputted thereto and for inputting the n digital picture element data into the multiplexor array.

5. The digital-type liquid crystal display panel driving circuit of claim 1, 2, 3 or 4, further including:

an output amplifier array provided between said digital to analog converter array and the demultiplexor array.

6. The digital-type liquid crystal display panel driving circuit of claim 1, 2, 3, 5 or 5, wherein the multiplexor array and demultiplexor array include MOS transistors.

7. The digital-type liquid crystal display panel driving circuit of claim 1, 2, 3, 4, 5 or 6, wherein a selecting time of the demultiplexor array is equal to k/n.

8. A method for driving a digital-type liquid crystal display panel comprising the steps of :

selecting k digital picture element data from n digital picture element data;

converting the k digital picture element data from the multiplexor array into k analog picture element signals;

selecting k of n data lines; and

transferring the k analog picture element signals from the digital to analog converter onto the selected k data lines.

9. The method of claim 8 further including the steps of:

temporarily storing n digital picture element data; and

inputting the n digital picture element data into the multiplexor array.

10. The method of claim 8 or 9 further including the steps of:

amplifying the output of the digital to analog converter.

11. The method of claim 8, 9 or 10 where the step of selecting k of n data lines includes the step of:

selecting k of n data lines a time equal to k/n.

12. A digital-type liquid crystal display panel substantially as hereinbefore described with reference to and/or substantially as illustrated in Fig. 2 and/or 3 of the accompanying drawings.

13. A method for driving a digital-type liquid crystal display panel, substantially as hereinbefore described with reference to and/or substantially as illustrated in Fig. 2 and/or 3 of the accompanying drawings.

The Patent Office

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Application No: GB 9810599.2 **Examiner:** Andrew Fearnside
Claims searched: 1-13 **Date of search:** 27 July 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): G5C (CHB)

Int Cl (Ed.6): G09G 3/36

Other: Online: WPI, JAPIO Databases.

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP0264918 A2	(CASIO) See fig. 12.	
A	WO 95/19658	(F.P.D TECHNOLOGY, INC.) See fig. 2	
Y	WO 94/16428	(YUEN FOONG) See line 6 of page 3, lines 29-35 of page 5 and figs. 1 and 2.	1,2,3,4,5, 6,8,9,10
Y	US 5170158	(TOSHIBA) See cols. 2, 8 & 9 and fig. 15	1,2,3,4,5, 6,8,9,10

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.